

Refine Search

Search Results -

Terms	Documents
(709/253 712/32 710/306 710/315 710/100 710/313 710/52 710/305 710/5 710/33).ccls.	6870

Database:

US Pre-Grant Publication Full-Text Database

US Patents Full-Text Database

US OCR Full-Text Database

EPO Abstracts Database

JPO Abstracts Database

Derwent World Patents Index

IBM Technical Disclosure Bulletins

Search:

L1

Refine Search

Recall Text

Clear

Interrupt

Search History

DATE: Tuesday, June 21, 2005 [Printable Copy](#) [Create Case](#)

<u>Set Name</u> side by side	<u>Query</u>	<u>Hit Count</u>	<u>Set Name</u> result set
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
<u>L1</u>	710/306,315,100,313,52,305,5,33;712/32;709/253.ccls.	6870	<u>L1</u>

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L1 and L2	33

Database:

US Pre-Grant Publication Full-Text Database
 US Patents Full-Text Database
 US OCR Full-Text Database
 EPO Abstracts Database
 JPO Abstracts Database
 Derwent World Patents Index
 IBM Technical Disclosure Bulletins

Search:

L3

Refine Search

Recall Text

Clear

Interrupt

Search History

 DATE: Tuesday, June 21, 2005 [Printable Copy](#) [Create Case](#)

Set Name Query

side by side

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

Hit Count Set Name

result set

<u>L3</u>	11 and L2	33	<u>L3</u>
<u>L2</u>	bridge same "state machine" same processor	142	<u>L2</u>
<u>L1</u>	710/306,315,100,313,52,305,5,33;712/32;709/253.ccls.	6870	<u>L1</u>

END OF SEARCH HISTORY

EAST - [Untitled1:1]

File View Edit Tools Window Help

☐ Drafts
☐ Pending
☒ **Active**
☐ L1: (12) "state machine"
☐ L2: (685) "state machine"
☐ L3: (46) 12 and (processor
☐ L4: (342) "state machine"
☐ L5: (23) 14 and (processor
☐ Failed
☐ Saved
☐ Favorites
☐ Tagged (0)
☐ UDC
☐ Queue
☐ Trash

☒ Plurals
☒ Highlight all hit terms initially

Default operator:

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comment	Error	Definit	Er
1	BRS	L1	12	"state machine" same mode same "real time"	USPA T	2005/05/3 1 15:47				
2	BRS	L2	685	"state machine" same mode same transfer\$4	USPA T	2005/05/3 1 15:49				
3	BRS	L3	46	12 and (processor same "buffer memory")	USPA T	2005/05/3 1 15:50				
4	BRS	L4	342	"state machine" same mode same (transfer\$4	USPA T	2005/05/3 1 15:49				
5	BRS	L5	23	14 and (processor same "buffer memory")	USPA T	2005/05/3 1 15:50				

EAST - [Untitled1:1]

File View Edit Tools Window Help

☐ Drafts
☐ Pending
☒ Active
 L1: (12) "state machine
 L2: (685) "state machir
 L3: (46) 12 and (proces
 L4: (342) "state machir
 L5: (23) 14 and (proces
☐ Failed
☐ Saved
☐ Favorites
☐ Tagged (0)
☐ UDC
☐ Queue
☐ Trash

Search List Browse Queue Clear
 DBs USPAT ☒ Plurals
 Default operator: OR ☐ Highlight all hit terms initially

14 and (processor same "buffer memory")

☒ BRS form ☒ IS&R form ☐ Image ☐ Text ☐ HTML

	U	I	Document ID	Issue Dat	Pages	Title	Current OR	Current X
1	<input type="checkbox"/>	<input type="checkbox"/>	US 6717576 B1	20040406	393	Deferred shading graphics pipeline proce	345/419	345/506; 345/522
2	<input type="checkbox"/>	<input type="checkbox"/>	US 6597363 B1	20030722	116	Graphics processor with deferred shading	345/506	345/545; 345/563
3	<input type="checkbox"/>	<input type="checkbox"/>	US 6564071 B1	20030513	17	Transmission of data over a radio frequency	455/557	714/749
4	<input type="checkbox"/>	<input type="checkbox"/>	US 6336180 B1	20020101	209	Method, apparatus and system for managing vir	712/34	711/206; 711/207
5	<input type="checkbox"/>	<input type="checkbox"/>	US 6323867 B1	20011127	17	Parsing graphics data structure into command	345/522	710/52
6	<input type="checkbox"/>	<input type="checkbox"/>	US 6268875 B1	20010731	23	Deferred shading graphics pipeline proce	345/506	345/422
7	<input type="checkbox"/>	<input type="checkbox"/>	US 6229553 B1	20010508	23	Deferred shading graphics pipeline proce	345/506	345/419; 345/426
8	<input type="checkbox"/>	<input type="checkbox"/>	US 5878217 A	19990302	10	Network controller for switching into DMA mode	709/212	709/236
9	<input type="checkbox"/>	<input type="checkbox"/>	US 5754889 A	19980519	40	Auto write counter for controlling a multi-sec	710/56	710/260; 712/220
10	<input type="checkbox"/>	<input type="checkbox"/>	US 5701450 A	19971223	21	System including ATA sequencer microprocesso	712/245	710/36; 711/118
11	<input type="checkbox"/>	<input type="checkbox"/>	US 5687389	19971111	40	System for controlling	710/5	365/50;

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End of Result Set

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L1: Entry 1 of 1

File: USPT

Nov 5, 2002

US-PAT-NO: [6477609](#)

DOCUMENT-IDENTIFIER: US 6477609 B1

TITLE: Bridge state-machine progression for data transfers requested by a host bus and responded to by an external bus

DATE-ISSUED: November 5, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Reiss; Loren B.	Raleigh	NC		
Sexton; Bonnie C.	Cary	NC		
Shiel; D. Adam	Eau Claire	WI		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Koninklijke Philips Electronics N.V.	Eindhoven			NL	03

APPL-NO: 09/ 495043 [\[PALM\]](#)

DATE FILED: January 31, 2000

INT-CL: [07] [G06](#) [F](#) [13/00](#)

US-CL-ISSUED: 710/306; 710/100, 710/107, 710/313, 710/260

US-CL-CURRENT: [710/306](#); [710/100](#), [710/107](#), [710/260](#), [710/313](#)

FIELD-OF-SEARCH: 710/107, 710/100, 710/305, 710/306, 710/313, 710/314, 710/315, 710/260, 710/267, 710/268

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

[Search Selected](#)[Search ALL](#)[Clear](#)

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/> 5943500	August 1999	Maguire et al.	710/260

ART-UNIT: 2181

PRIMARY-EXAMINER: Thai; Xuan M.

ATTY-AGENT-FIRM: Zawitski; Peter

ABSTRACT:

An expansion module for a Handspring Visor (which conforms to the Springboard bus specification) includes a multi-master AMBA Advanced System Bus (ASB). Optionally, an Arm7 processor is attached to this bus via an Arm7 to ASB interface as one master. The Springboard bus of the visor is coupled to the ASB bus via a Springboard-to-ASB-bus bridge. This bridge comprises a protocol translator and a second Arm7 to ASB interface. The protocol translator translates bi-directionally between the Springboard bus protocol and the Arm7TDMI protocol. The translator includes an interface to the Springboard bus and a state machine. The state machine coordinates data transfers between the buses. The state machine also monitors signals indicating when each of said buses begins to treat a data transfer as complete so that the data transfer can be validated or flagged as an error condition. A programmable counter adjusts maximum counts to compensate for different clock frequencies in measuring a write-wait state duration to ensure valid writes from the Visor to the ASB bus. Using this basic design framework, a developer of Springboard expansion modules can take immediate advantage of the performance and the variety of peripherals available for the ASB bus. Furthermore, using the same translator and merely changing the interface to the external bus, a Springboard developer can take advantage of peripherals developed for other external buses as well.

10 Claims, 10 Drawing figures

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L3: Entry 14 of 33

File: USPT

Oct 14, 2003

US-PAT-NO: 6633944

DOCUMENT-IDENTIFIER: US 6633944 B1

TITLE: AHB segmentation bridge between busses having different native data widths

DATE-ISSUED: October 14, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Holm; Jeffrey J.	Eden Prairie	MN		
Emerson; Steven M.	Chanhassen	MN		
Kirkwood; Matthew D.	West St. Paul	MN		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
LSI Logic Corporation	Milpitas	CA			02

APPL-NO: 10/ 000716 [\[PALM\]](#)

DATE FILED: October 31, 2001

INT-CL: [07] [G06](#) [F](#) [13/00](#)

US-CL-ISSUED: 710/306; 710/100, 710/52, 370/402

US-CL-CURRENT: [710/306](#); [370/402](#), [710/100](#), [710/52](#)

FIELD-OF-SEARCH: 710/100, 710/52, 710/310, 710/107, 710/315, 710/307, 710/305, 710/306, 370/402, 370/916

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	4309754	January 1982	Dinwiddie, Jr.	
<input type="checkbox"/>	5590287	December 1996	Zeller et al.	
<input type="checkbox"/>	5664117	September 1997	Shah et al.	
<input type="checkbox"/>	5768545	June 1998	Solomon et al.	
<input type="checkbox"/>	6065093	May 2000	Dell et al.	
<input type="checkbox"/>	6076128	June 2000	Kamijo et al.	
<input type="checkbox"/>	6101565	August 2000	Nishtala et al.	
<input type="checkbox"/>	6147672	November 2000	Shimamoto	

ART-UNIT: 2181

PRIMARY-EXAMINER: Ray; Gopal C.

ATTY-AGENT-FIRM: Maiorana PC; Christopher P.

ABSTRACT:

A bus bridge generally comprising a first interface, a second interface, a plurality of registers and a controller. The first interface may be connectable to a first bus having a first data width. The second interface may be connectable to a second bus having a second data width narrower than the first data width. The plurality of registers may be configured to buffer (i) data, (ii) an address, and (iii) a plurality of control signals between the first bus and the second bus. The controller configured to control the registers.

20 Claims, 4 Drawing figures

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L3: Entry 31 of 33

File: USPT

May 13, 1997

US-PAT-NO: 5630094

DOCUMENT-IDENTIFIER: US 5630094 A

**** See image for [Certificate of Correction](#) ****

TITLE: Integrated bus bridge and memory controller that enables data streaming to a shared memory of a computer system using snoop ahead transactions

DATE-ISSUED: May 13, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hayek; George	Cameron Park	CA		
Oztaskin; Ali S.	Beaverton	OR		
Langendorf; Brian	El Dorado Hills	CA		
Young; Bruce	Tigard	OR		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA			02

APPL-NO: 08/ 375972 [\[PALM\]](#)

DATE FILED: January 20, 1995

INT-CL: [06] [G06 F 13/00](#), [G06 F 13/40](#), [G06 F 3/00](#)

US-CL-ISSUED: 395/473; 395/474, 395/494, 395/308, 395/309, 395/872

US-CL-CURRENT: [711/146](#); [710/310](#), [710/52](#), [711/147](#), [711/167](#)

FIELD-OF-SEARCH: 395/473, 395/474, 395/494, 395/306, 395/308, 395/309, 395/872, 395/464, 395/468

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	5072369	December 1991	Theus et al.	395/473
<input type="checkbox"/>	5195089	March 1993	Sindhu et al.	370/85.1
<input type="checkbox"/>	5317718	May 1994	Jouppi	395/464
<input type="checkbox"/>	5325503	June 1994	Stevens et al.	395/473
<input type="checkbox"/>	5335335	August 1994	Jackson et al.	395/473
<input type="checkbox"/>	5341487	August 1994	Derwin et al.	395/473
<input type="checkbox"/>	5353415	October 1994	Wolford et al.	395/306

<input type="checkbox"/> <u>5355467</u>	October 1994	MacWilliams et al.	395/473
<input type="checkbox"/> <u>5379384</u>	January 1995	Solomon	395/308
<input type="checkbox"/> <u>5420991</u>	May 1995	Konigsfeld et al.	395/375
<input type="checkbox"/> <u>5499355</u>	March 1996	Krishnamohan et al.	395/464

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
6-37768	February 1994	JP	

ART-UNIT: 232

PRIMARY-EXAMINER: Gossage; Glenn

ATTY-AGENT-FIRM: Blakely, Sokoloff, Taylor & Zafman

ABSTRACT:

A computer system having an integrated bus bridge and memory controller circuit and method for enabling access to a shared memory with high bandwidth data streaming are disclosed. The integrated bus bridge and memory controller circuit performs a series of snoop ahead transactions over a first bus during access transactions to the shared memory that originate over a second bus and thereby enables high bandwidth data streaming on the second bus. The integrated bus bridge and memory controller circuit includes a peripheral write buffer that buffers write data received over the second bus and that stores a snoop done flag for the write data that indicates whether a corresponding snoop ahead transaction for the write data is complete. The integrated bus bridge and memory controller circuit further includes a peripheral read prefetch buffer that prefetches read data during read transactions over the second bus only after a corresponding snoop ahead transaction for the read data is complete.

8 Claims, 5 Drawing figures

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